

## PATENT ABSTRACTS OF JAPAN

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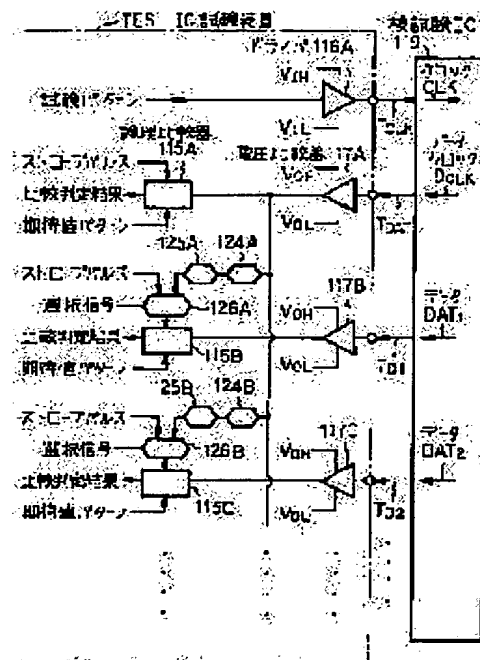
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## (54) IC TESTING APPARATUS

## (57)Abstract:

**PROBLEM TO BE SOLVED:** To simply generate a test program by extracting a data clock pulse, delaying the extracted pulse within the expected range of time and then supplying a timing setting pulse to a logical comparator through conversion to the strobe pulse.

**SOLUTION:** Selection circuits 126A, 126B are switched to select the pulses output from the timing setting circuits 125A, 125B and to supply such pulses to each logical comparators 115B, 115C. The expectation time up to the output from the timing of data clock DCLK is set to the timing setting circuits 125A, 125B. A pulse is also given in the timing after elapse of expectation time from the rise or fall timing of the data clock DCLK is given to the logical comparators 115B, 115C. Signals of data DAT1, DAT2 output from the data terminals TD1, TD2 of the IC119 to be tested are compared and the logical value and expectation value pattern when the above signals exist are compared logically.



## LEGAL STATUS

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